PCL-850 CLOCK GENERATOR

User' Manual

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1. Functional outline

As a signal source, desired clock signals can be generated with 1Hz resolution in an extremely wide band of 1MHz to 850MHz. Wideband signals up to 850MHz are generated by PLL multiplication of the signal generated by a 32-bit DDS (direct signal synthesizer). The frequency is set with asynchronous serial data. Also, the frequency can be easily set by selecting CHs saved in the incorporated 64CH memory with parallel data.

2. Specifications

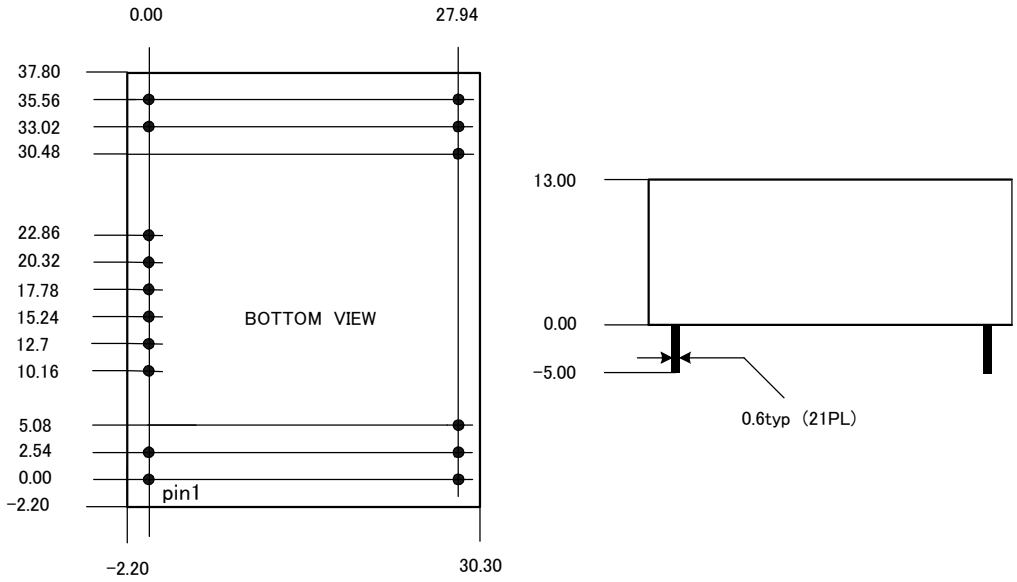
2-1. Electrical specifications

Power supply voltage	+3.3V±5%
Consumption current	250mA or less
Output level	LVPECL differential output (3.3V)
Output frequency range	1MHz - 850MHz
Frequency resolution	1Hz
Output waveform duty	50%±20%
Frequency accuracy	±20ppm(0 - 50℃)
Jitter	1MHz - 400MHz ±30pSrms
	400MHz - 850MHz ±50pSrms
	(Cycle to Cycle Jitter)
Spurious level	1MHz - 100MHz -45dB or more
	400MHz - 820MHz -32dB or more
Frequency control	Serial input two signal lines
	9600bps, 8 bits
	No parity, 1 stop bit
	ASCII 9-digit numerical data + line feed code
Memory CH selection	Parallel input eight signal lines
	6 bits; selection signals (64CH)
	1 bit; SET signal
Frequency setting time	Within 5mS
	Time between transferring a delimiter code and obtaining the set frequency in the case of serial data.
	Time between giving a SET signal and obtaining the set frequency in the case of memory CH selection.
Outer dimensions	40x32.5x13 (mm)

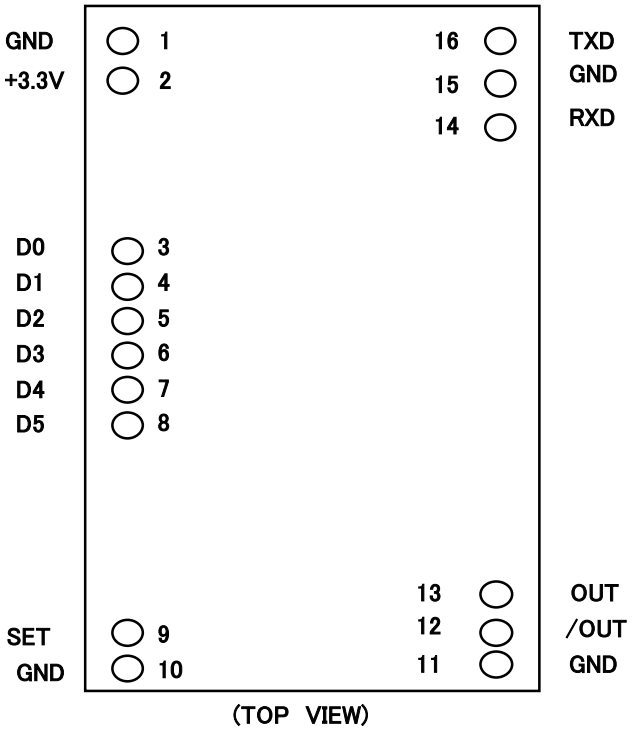
2-2. Environmental conditions

Operating temperature range	0℃~50℃
Storage temperature range	-30℃~+70℃

3. Outer dimensions



4. Pin assignments



5. Pin names and descriptions

Pin No.	Name	Description
1	GND	Power supply/signal GND.
2	+3.3V	Power supply pin, to which +3.3V±5% should be supplied.
3	D0	Memory CH selection signal. Input of signal selection bit 0 (2^0).
4	D1	Memory CH selection signal. Input of signal selection bit 1 (2^1).
5	D2	Memory CH selection signal. Input of signal selection bit 2 (2^2).
6	D3	Memory CH selection signal. Input of signal selection bit 3 (2^3).
7	D4	Memory CH selection signal. Input of signal selection bit 4 (2^4).
8	D5	Memory CH selection signal. Input of signal selection bit 5 (2^5).
9	SET	Set signal for memory CH selection. As it is pulled up (10KΩ) internally, the frequency in the memory CH selected by D0 - D5 is set by connecting it to GND. Data is loaded on the falling edge.
10	GND	Power supply/signal GND.
11	GND	Power supply/signal GND.
12	/OUT	PECL differential output terminal.
13	OUT	PECL differential output terminal.
14	RXD	Asynchronous serial data input pin. The level is 3.3V CMOS. When not in use, open it.
15	GND	Power supply/signal GND.
16	TXD	Asynchronous serial data output pin. The level is 3.3V CMOS. When not in use, open it.

6. Control by serial data

How to set from a PC serial port (RS-232C) is explained below.

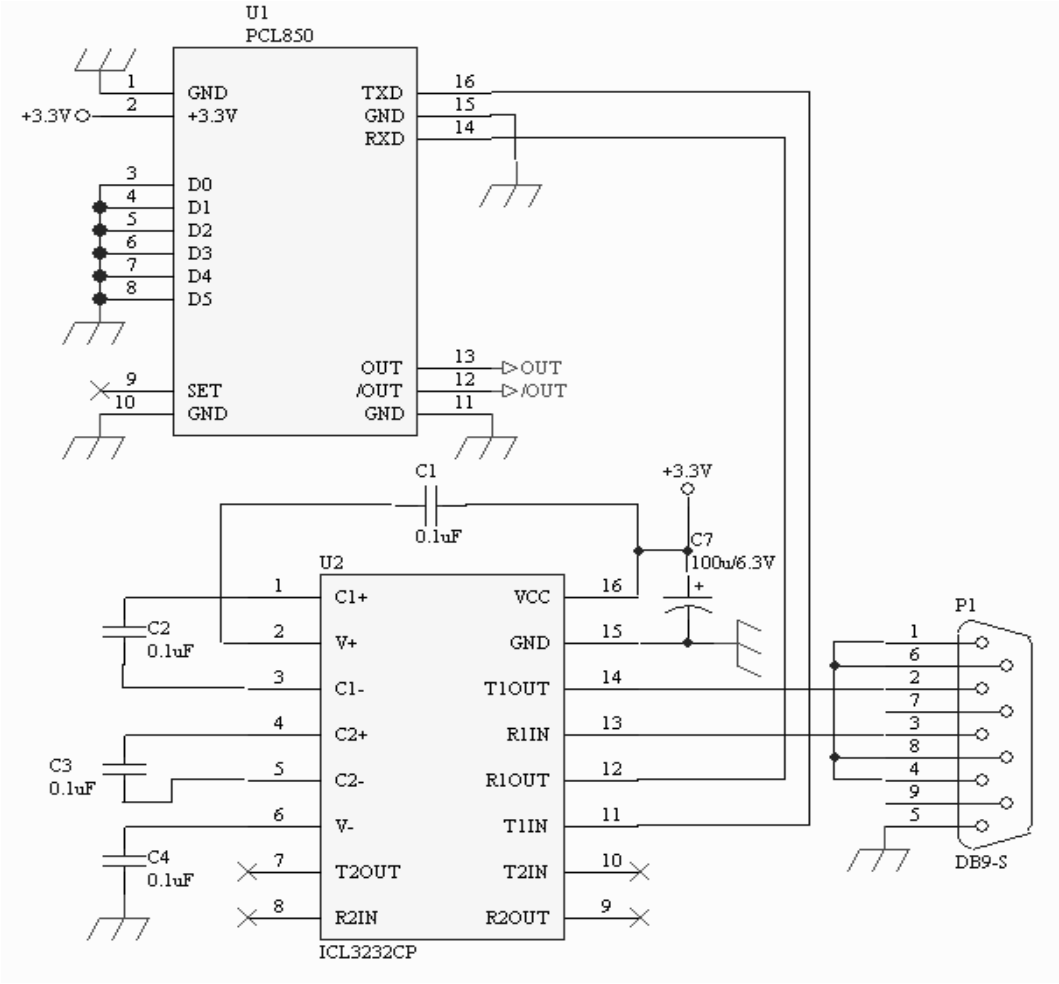
6-1. Communication specifications

Communication speed	9600bps
Data bit	8 bits
Parity	None
Stop bit	1 bit
Flow control	None
Level	3.3V CMOS

6-2. RS-232C connection

The electric signal level of PCL-850 serial communications is 3.3V CMOS, which cannot be directly connected to a PC serial port, etc. (RS-232C level).

Level conversions between RS-232C and 3.3V CMOS are made via the level converter as shown in the following figure.



Note: The U2 level conversion IC is ICL3232CP manufactured by INTERSIL. The other ICL32XX series of level conversion ICs are also usable.

6-3. Command definitions

Character strings enclosed in double quotation marks " " mean ASCII codes, and CR and LF, which are control codes, mean 0D (hex) and 0A (hex).

If any invalid command is input, "INVALID DATA" LF CR "*" is returned.

All characters used for input should be uppercase. If a normal command is input, "*" is returned. Also, the input data is echoed back.

6-3-1. Frequency setting command

For frequency setting, inputs can be made in MHz, KHz, and Hz.

(1) Setting in MHz

For setting 123MHz, input the following data.

"123M" CR

In this case, all the data below 100KHz is set to "0."

(2) Setting in KHz

For setting 123456KHz, input the following data.

"123456K" CR

In this case, all the data below 100Hz is set to "0."

(3) Setting in Hz

For setting 123456789Hz, input the following data.

"123456789" CR

6-3-2. SAVE command

By inputting "SAVE" CR, the currently set frequency is saved in nonvolatile RAM. The saved frequency is output when the power is turned on again.

By inputting "SAVE xxx yyy..." CR, the frequency can be saved in the specified memory CH.

Here, xxx is a memory address of 64CH specified by 0 - 63 at the maximum.

yyyyyy... is the frequency data explained in 6-3-1.

For saving a frequency of 123MHz in memory CH address 0, input the following data.

"SAVE 0 123M" CR

For saving a frequency of 123456KHz in memory CH address 63, input the following data.

"SAVE 63 123456K" CR

6-3-3. READ command

By inputting "READ" CR, the currently saved data in all memory CHs is output. The response is as follows:

"fffffffff" CR LF
"00 fffffffff" CR LF
"01 fffffffff" CR LF
"02 fffffffff" CR LF
.
.
.
"63 fffffffff" CR LF
"*"

"fffffffff" on the first line is the default frequency to be output at power-on. On the second line to the 121st line frequency data is saved in the memory CHs.

Here, "fffffffff" is the output frequency in each memory CH displayed in Hz.

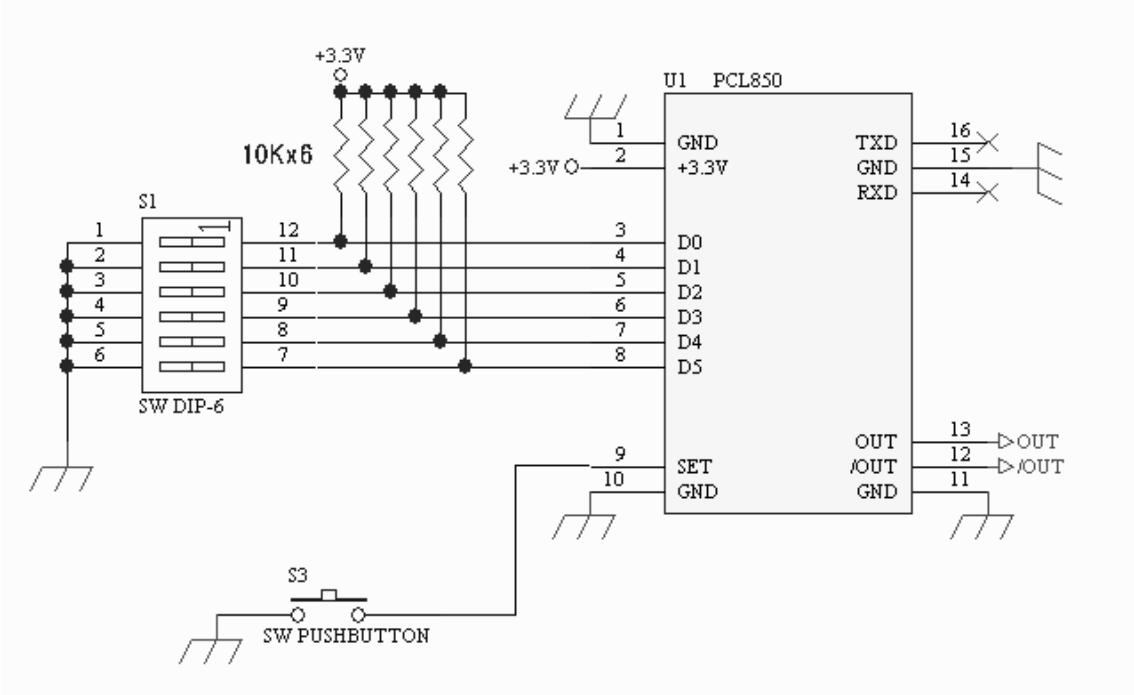
6-4. Caution for setting data consecutively

In the case of switching frequencies at high speed, data may drop out because the PCL850 does not perform flow control. Upon completion of processing by sending a frequency setting command in 6-3-1, the prompt "*" is returned; therefore, confirm the receiving of this prompt, and then send the next frequency setting command.

7. Memory CH selection by parallel data

It is designed so that frequency data saved in the maximum 64CH memory can be easily set by seven selection signals and one SET signal.

7-1. Example of SW connection circuit



Remarks: Only the SET signal is pulled up internally.

When not using D0 - D5, connect them to VCC or GND.

The input data of D0 - D5 is loaded on the falling edge of SET.

When not using RXD and TXD, open them.

8. Shipping inspection

8-1. Electrical inspection

100% inspection shall be performed for the electrical specifications in 2-1.

8-2. Appearance inspection

Inspection shall be performed for contamination and bends in pins.

9. Soldering conditions

Perform soldering at a temperature of 260℃ or less within 10 seconds.

10. Warranty

If any defect is found due to the manufacturer's improper production or design within one year after delivery, repair or replacement shall be performed at the manufacturer's responsibility.

11. Other

11-1. This product, which employs a CMOS device, may be easily damaged by static electricity.

11-2. Keep in mind that immersion cleaning is not allowed.

11-3. Special damp proof control is not necessary.

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